Embedded Software Development on Virtual Platforms – Are We Ready For Industrial Deployment?

One-day industrial workshop
in-conjunction with Embedded World 2013

Organizers:
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Motivation:
Embedded software development process and methodologies aims today mainly at simple single-core platforms and is detached from performance characteristics of the underlying hardware and hardware-dependent software. Due to power and performance constraints today's most advanced platforms are dominated by multi-core and heterogeneous architectures. To efficiently exploit these platforms in the software development process we need to carefully consider the platform artefacts, performances, characteristics, features and strengths.

Current software development process is not efficient anymore because of:

- Long overall development time of software starting late after the hardware platform is available
- Difficult debugging, testing and validation of software on complex hardware platforms
- Optimized usage of available resources (hardware, low-level software, …)
- Cost of optimization, re-spins, bug fixing in both software and hardware

Virtual Platforms offer a viable and powerful solution to the above weaknesses.

Description:
Development and integration of embedded software executing on a hardware platform is increasingly becoming a key factor in product differentiations well as in its final market success or failure. Not only does the software development process determine the overall product functionality, it also significantly influences its entire development time. If the software is finished too late then the entire product can fail.

In addition software complexity is growing and consumes significant development and verification time. Add to this the trend towards multi-core architectures today, which makes them challenging to analyze and debug, and it should come as no surprise that recent studies show that software development effort already surpasses the effort spent on hardware for a typical 90nm SoC design. Furthermore, software becomes an integral part of any system verification concept, as only the combination of hardware and software allows verifying system functionality.

With an ever growing system complexity the industry needs to apply new concepts, paradigms and methods for embedded software development and hardware/software system validation that will be able to tackle with the problems of quality and correctness, providing significant gain in the design productivity and shorten time to market.

It is the belief that such a new way of development will be based on **embedded software development on virtual platforms** that offer a set of executable models, that can be used by software developers for design, structuring and optimization as well as verification and validation purposes. The concept of system virtualization has been around for almost a decade, during which time the industry started to learn how to build and apply these technologies. Topics of controversy have been the necessary accuracy vs. possible

simulation performance, the need for a system-level IP eco system, and the move from tool-specific simulation paradigms towards public standards.

This workshop will cover the state-of-the-art of embedded software development on virtual platforms. This includes technologies and tool environments for building, executing and distributing virtual platforms. It will address existing and upcoming industry standards. Significant room will be given to cover user experience, both from those building virtual platforms, as well as from those deploying virtual platforms for embedded software development, or software-driven system validation.

Lessons learned, problems solved, remaining issues will be shared with the participants.

Target Audience:

- Embedded software developers: application, hardware dependent software, and driver developers
- Embedded system developers
- Software verification engineers
- Virtual platform developers

Workshop Structure and Agenda	
9:30-9:35	**Introduction** Agenda Presentation
9:35-10:45	**Virtual Platform Concepts Introduction and Typical Use Cases** *This session will provide an overview on concepts in Virtual Platforms including modeling, interfaces, flows, visibility o platform details, observability, debugging capabilities, typical use cases…* The session will help participants to learn about the rationales why the Virtual Platform concept has been developed, what is available to the software developer who starts the application development, what are the technical and economic advantages of using virtual platforms in the embedded software development process as well as features like: usability: debugging, verification, traceability, etc. Presentations: - Virtual Platform Introduction: Platform Simulation Technologies *Eugenio Villar, University of Cantabria, Spain* - Performance and Energy Modeling and Analysis in COMPLEX Virtual Platform *Frank Oppenheimer, OFFIS, Germany*
10:45-11:00	**Coffee Break**
11:00-12:00	**Embedded World Keynote**
12:00-13:30	Lunch and Networking
13:30-15:30	**Virtual Platform Integration and Provision** Virtual Platform Verification *Michael Bartley, Test & Verification Solutions, UK* *(remote presentation)* Using Virtual Plaforms for Efficient Software Development and Research *Patrik Ekström, Realtime Embedded, Sweden* Emul8 – A New Emulator for a Changing Industry Michael Gielda, Ant Micro, Poland Building Reusable Connectivity IP Blocks for Virtual Platform *Carsten Elgert, Evatronix, Germany*
15:30-16:00	**Poster Presentations** (Projects: COMPLEX, CRAFTERS, PAPP) + Coffee Break

16:00-16:30	**Embedded Software Development on Virtual Platform** FASTCUDA: Hardware/Software Co-design and FPGA Implementation for CUDA Kernels. *Florian Schäfer, FSResult GmbH, Germany*
16:30-17:30	Design Environment for Virtual Platform Modeling and Analysis *Frank Schirrmeister, System & Software Realization Group, Cadence Design Systems, USA* Towards Software Development on a Virtual Prototype with Unambiguous HW/SW Contract *Marleen Boonen, Methods2Business, The Netherlands*
17:30-18:00	**Panel** **Highlights and Lowlights for Virtual Platform Usage** Discussion between proponents of virtual platform solution (from software developers, EDA and platform providers) and traditional flow supporters.

Workshop Organisation:

In order to support the organization of the workshop the organizers will:

- Ensure the whole technical organization of the event: invitation of presenters, workshop agenda set-up, sessions structure

- Provide to the Embedded World organizers
  - Announcement messages for the workshop publicity and inclusion in the program and/or other materials
  - Detailed program information by defined deadlines
  - Cooperate on any organization and publicity action with the organizers

- Ensure publicity of the event to their own mailing lists (more than 22000 addresses world-wide) and web-pages to strengthen the visibility and impact of the workshop and Embedded World in general

- Provide to the workshop participants:
  - Workshop presentations on a USB key
  - Collaterals: printed workshop program, bags, pens, notepads, etc
  - Access to the web page where all updated presentations will be stored