Title:

"Towards embedded system development with unambiguous HW/SW contract"…

Paper Category: System Design & Verification, Functional Verification

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Abstract:

Software content in todays embedded systems is exploding and screams for a software-centric approach in embedded system design to increase engineering productivity, guarantee product quality and predict and control development costs. This requires that Semiconductor companies today have to deliver silicon including a working software stack to allow easy development and deployment of complex software applications.

What we often see is that it is not easy to bring the hardware and software together. The difficulty lies in avoiding mismatches between hardware and software because of misunderstandings between the hardware and software engineers. Therefore, an unambiguous HW/SW contract, which can be guaranteed for both the HW and the SW, is needed at the start.

Last year we presented the double paradigm shift that can be realized to design embedded systems by combining virtual prototyping using Cadence Virtual System Platform with formally proven model driven software generation using Verum®'s unique Software Design Automation platform.

This year's presentation will go one step further by demonstrating that it is possible to mathematically prove that the assumptions the software has about the hardware captured in the hardware / software contract hold for both the hardware and the software.

The challenge for this presentation will be to demonstrate how an unambiguous hardware / software contract should look for a realistic use case. We know that the software developed in Verum®'s ASD:Suite obeys the assumptions made about the hardware behavior when described in the interface models.

The real innovative part of this presentation lies in showing how the assumptions made about the hardware can be reflected in the SystemC models generated by the Cadence® virtual prototyping solution. Since the assumptions made about the hardware in the contract can still be wrong unless formally proven on the real RTL code, we will show that it is possible to translate them in formal properties (SVA, PSL) and mathematically prove them on the implemented hardware by using Cadence® Incisive Formal Verifier (IFV) solution.

In addition, we will demonstrate the recent advances in Cadence virtual prototyping solution - the new Eclipse based version of VSP. Again we will build our virtual prototype around the ARM® Fast models to guarantee the binary compatibility of the software and the required simulation speed (minimum 100 MIPS) to run and debug software.